

FIG. 1 is a block diagram of a receiver system 100. The receiver system 100 includes an antenna 102, a switch 105, a first receiver branch 101, a second receiver branch 103, a combiner 123, a deinterleave block 125, and a decode block 127.

FIG. 1
Prior Art

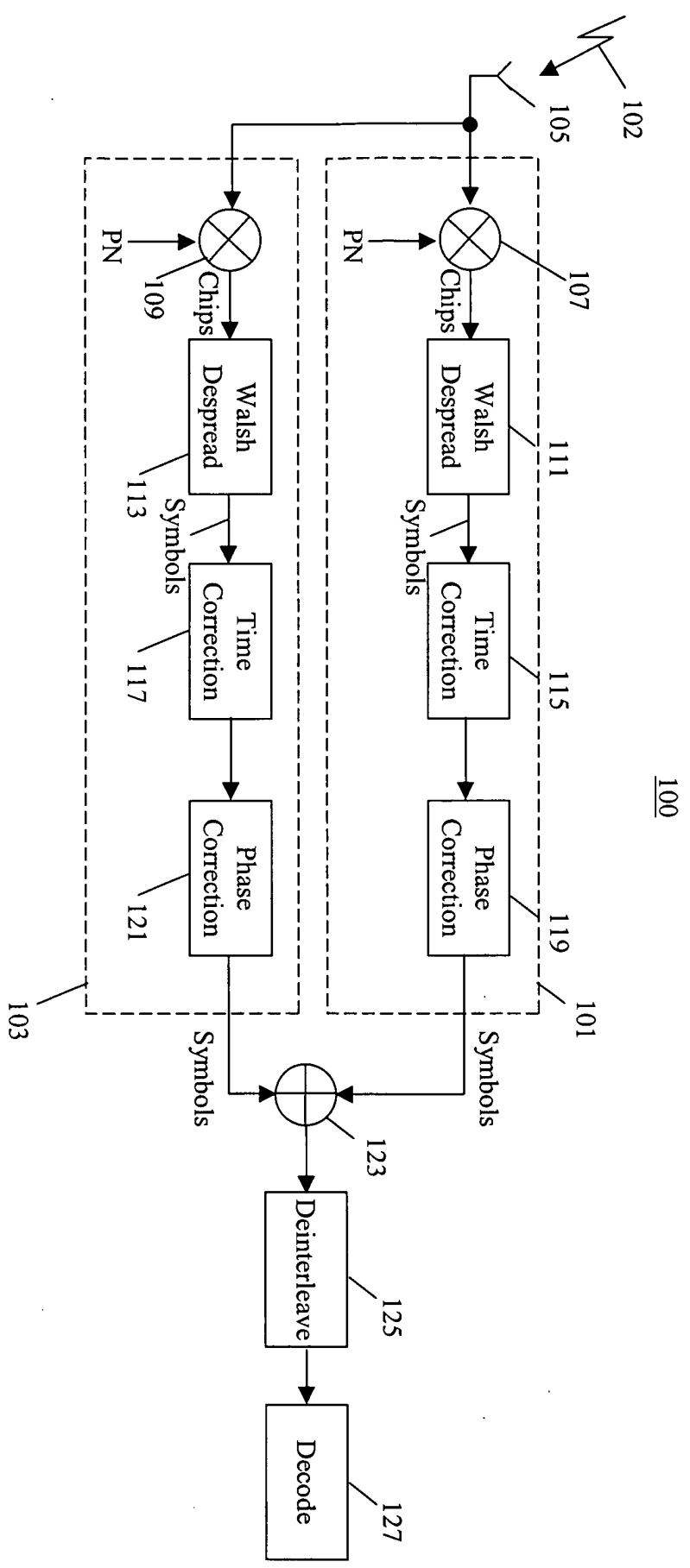
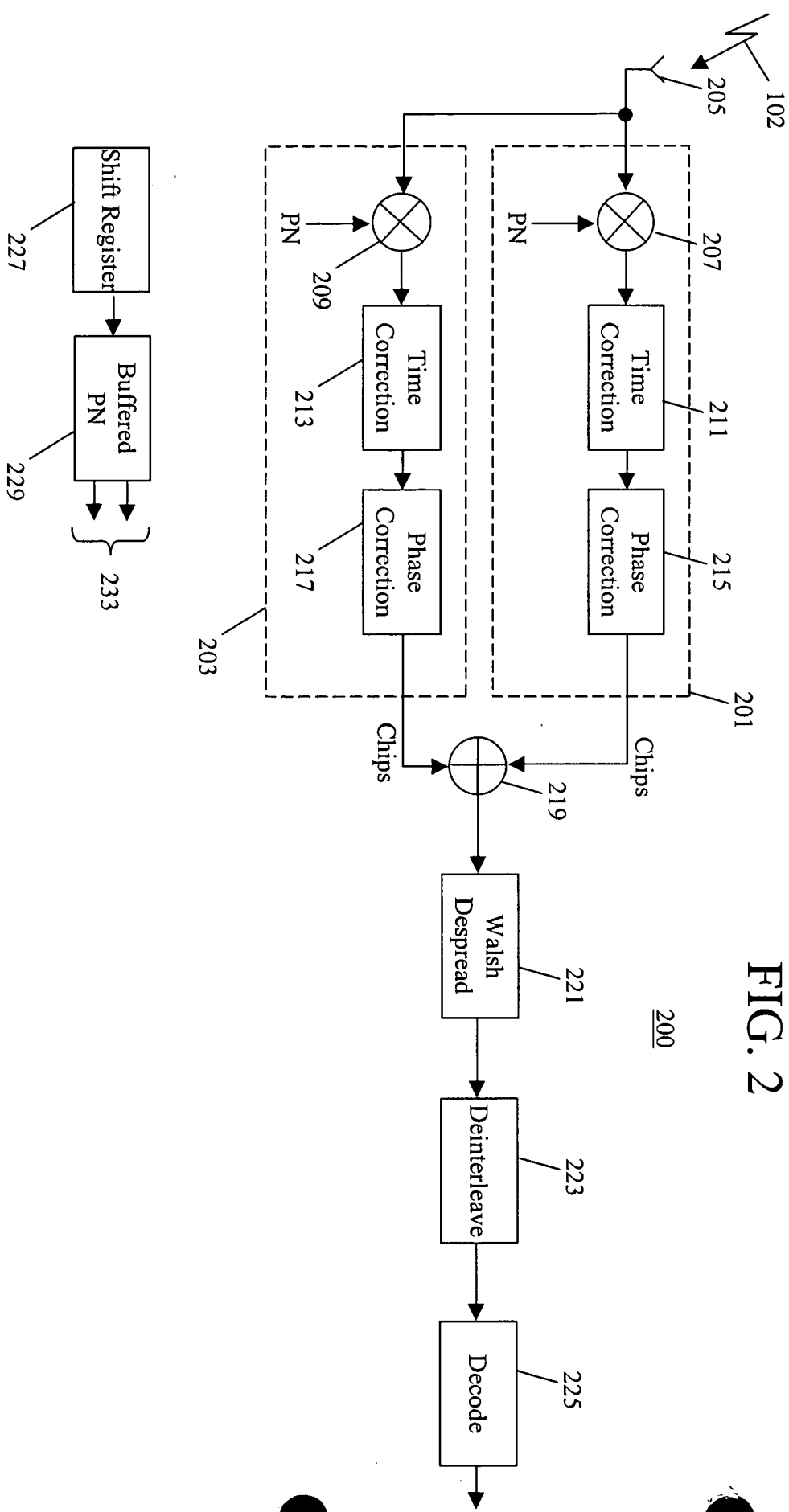


FIG. 2 is a block diagram of a receiver system 200. The receiver system 200 includes an antenna 102, a switch 205, a first correlator 207, a second correlator 209, a first time correction block 211, a second time correction block 213, a first phase correction block 215, a second phase correction block 217, a summing junction 219, a Walsh Despread block 221, a Deinterleave block 223, and a Decode block 225. The receiver system 200 also includes a Shift Register 227 and a Buffered PN block 229, which together form a PN sequence generator 233.

FIG. 2



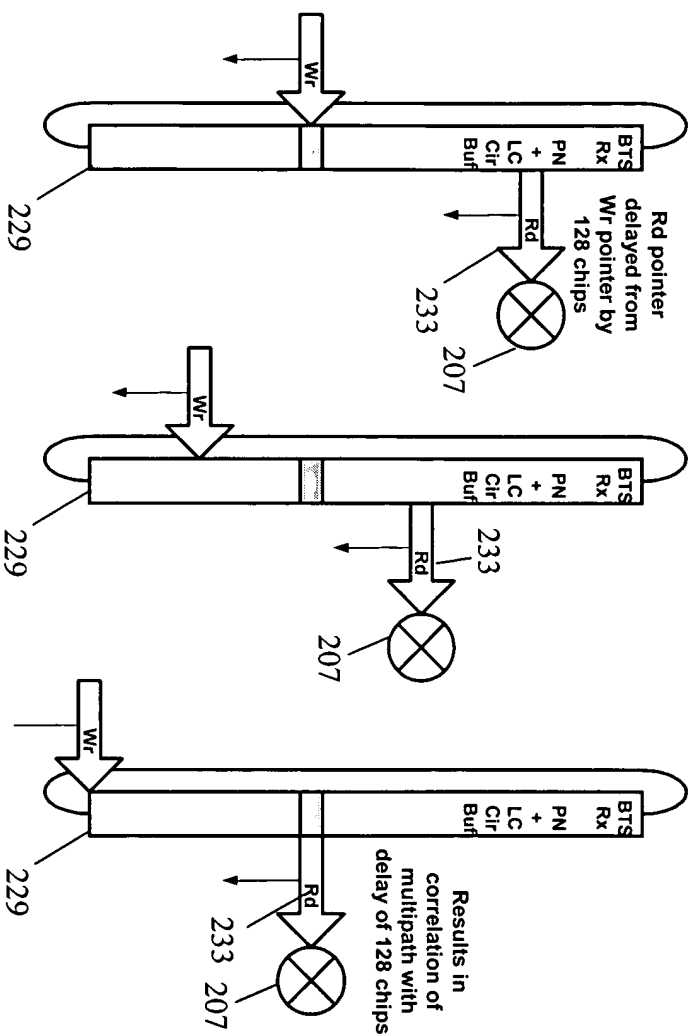


FIG. 3

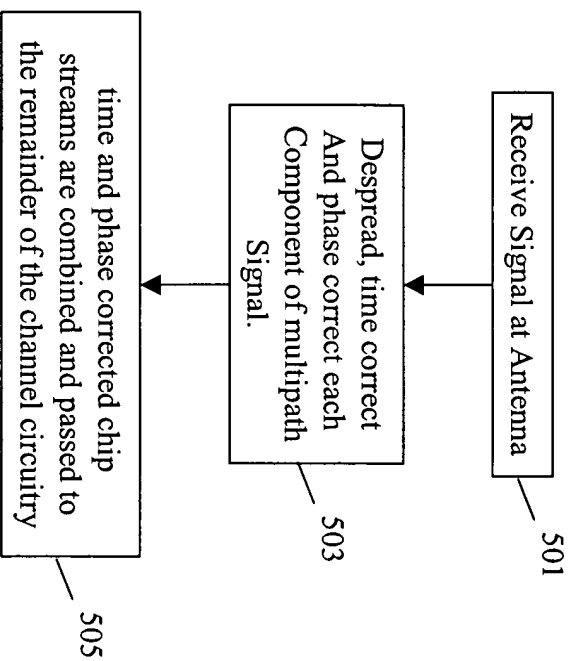


FIG. 5

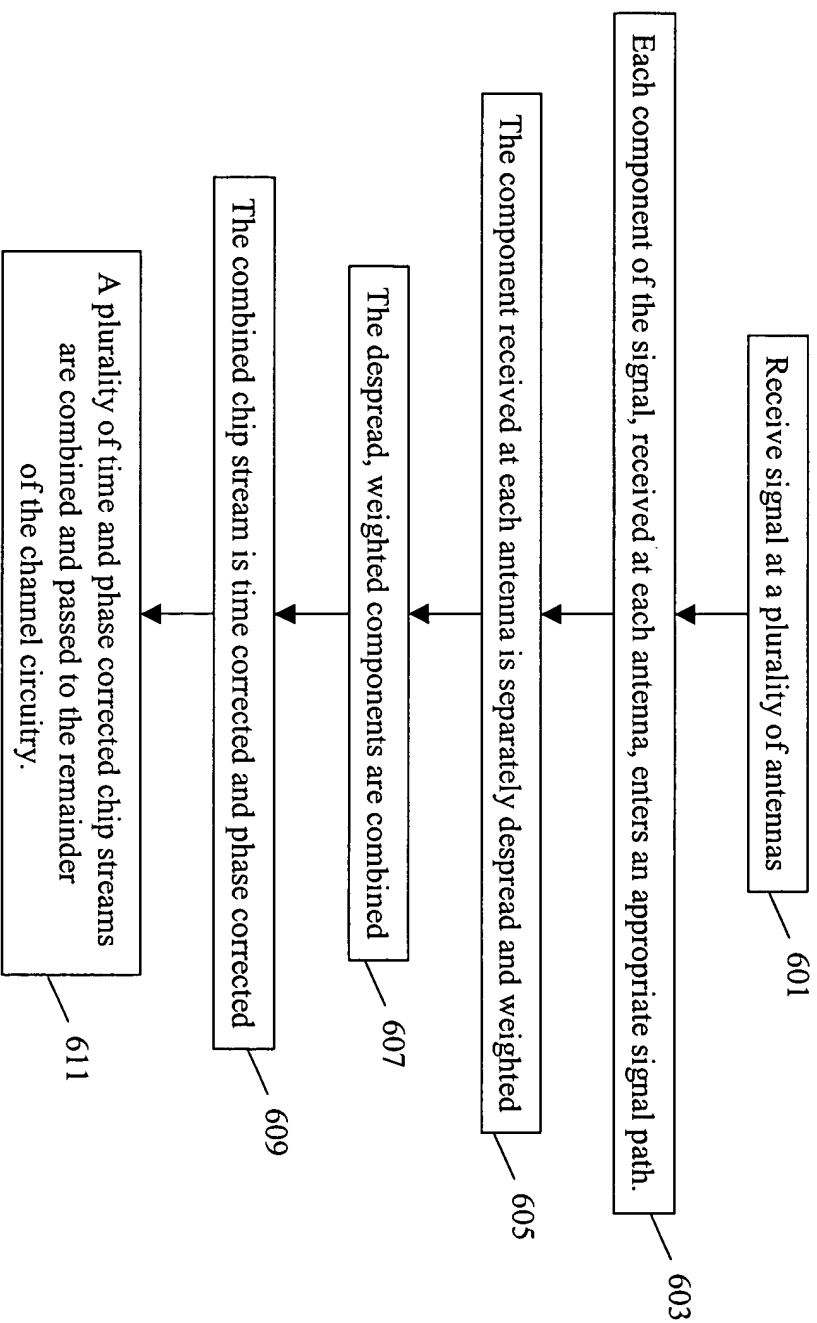


FIG. 6

FIG. 7 is a block diagram of a multi-user receiver system. The system includes an antenna (701) connected to a TDM S/P block (703). The TDM S/P block outputs 4TDM signals to multiple users (User 1, User 2, ..., User X2). Each user's signal path includes a series of multipliers (1.32fc) and a PN Read Pointer (713). The signals are then processed by a series of multipliers (1.64fc) and a final combine block (719). The output of the final combine block is fed into a Phase Corr block (725) and a Combine block (709). The Phase Corr block outputs 8,fc signals to the Combine block. The Combine block outputs 8,fc signals to a user (User 1). The system also includes a DLL (707) and a CE (708) block. The DLL block outputs 8,adv signals to the CE block. The CE block outputs 8,ge signals to the Combine block. The system is labeled FIG. 7.

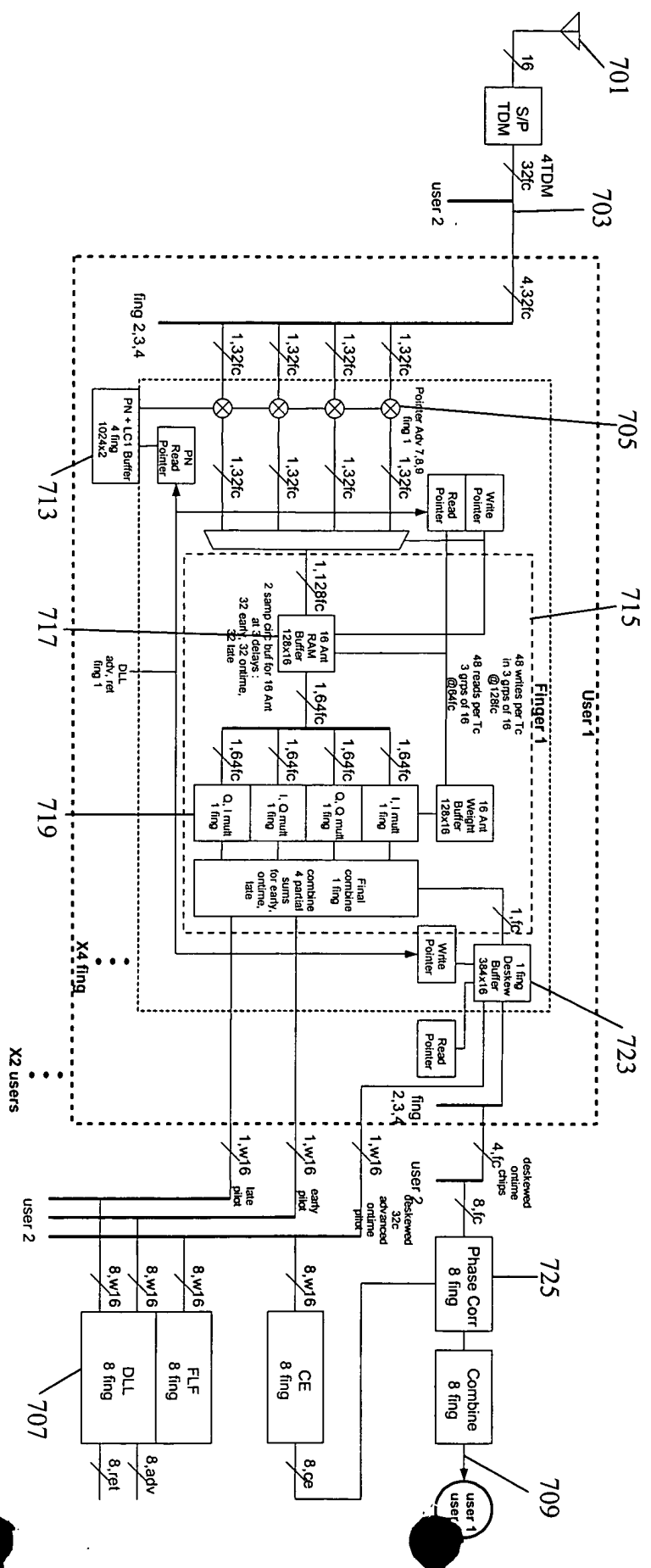


FIG. 7